1. A method for forming an interlevel dielectric (ILD) layer with improved gap filling comprising the steps of:

providing a semiconductor substrate having closely spaced gate electrodes;

forming sidewall spacers on said gate electrodes;

forming source/drain contact areas adjacent to said sidewall spacers;

forming a metal silicide layer on said gate electrodes and on said source/drain contact areas;

removing said sidewall spacers;

forming said interlevel dielectric layer over and between said gate electrodes and filling gaps between said gate electrodes on said substrate.

2. The method of claim 1, wherein said closely spaced gate electrodes are formed from a polysilicon layer deposited to a thickness of between about 1500 and 1800 Angstroms.

3. The method of claim 1, wherein said substrate includes lightly doped source and drain regions adjacent to said closely spaced gate electrodes and wherein said lightly doped source and drain regions are formed by ion implanting an N type dopant for N-channel

devices and ion implanting a P type dopant for P-channel devices.

4. The method of claim 1, wherein said sidewall spacers are formed by depositing a conformal chemical-vapor deposited insulating layer and anisotropically etching back to said semiconductor substrate, and resulting in an aspect ratio of said gaps between said gate electrodes of at least 6.0.

5. The method of claim 1, wherein said source/drain contact areas are formed by ion implanting an N^+ type dopant for N-channel devices and ion implanting a P^+ type dopant for P-channel devices.

6. The method of claim 1, wherein said metal silicide layer is formed on said gate electrodes and on said source/drain contact areas using a salicide process that uses a metal selected from the group that includes cobalt, nickel, and titanium.

7. The method of claim 1, wherein said metal silicide layer is formed to a thickness of between about 250 and 400 Angstroms.

8. The method of claim 1, wherein said sidewall spacers are silicon nitride and are completely removed using a hot phosphoric acid solution (H_3PO_4) and result in an aspect ratio of said gaps of about 1.4.

9. The method of claim 1, wherein said sidewall spacers are silicon oxide, and are completely removed using in-situ plasma etching in a high-density plasma etcher and result in an aspect ratio of said gaps of about 1.4.

10. The method of claim 1, wherein said sidewall spacers are partially removed to provide an aspect ratio of said gaps of between about 1.4 and 6.0.

11. The method of claim 1, wherein said interlevel dielectric layer is a phosphorus-doped silicon oxide deposited by chemical-vapor deposition to a thickness of at least about 9500 Angstroms.

12. The method of claim 11, wherein said interlevel dielectric layer includes a silicon nitride barrier layer having a thickness of about 600 Angstroms.

13. The method of claim 1, wherein said interlevel dielectric layer is a dielectric material having a low-dielectric constant.

14. A method for forming an interlevel dielectric (ILD) layer with improved gap filling comprising the steps of:

providing a semiconductor substrate having closely spaced polysilicon gate electrodes;

forming lightly doped source and drain regions adjacent to said polysilicon gate electrodes;

forming sidewall spacers on said polysilicon gate electrodes;

forming source/drain contact areas adjacent to said sidewall spacers;

forming a self-aligned metal silicide layer on said polysilicon gate electrodes and on said source/drain contact areas;

partially removing said sidewall spacers;

forming said interlevel dielectric layer over and between said polysilicon gate electrodes and filling gaps between said polysilicon gate electrodes on said substrate.

15. The method of claim 14, wherein said closely spaced polysilicon gate electrodes are formed from a

polysilicon layer deposited to a thickness of between about 1500 and 1800 Angstroms.

16. The method of claim 14, wherein said lightly doped source and drain regions are formed by ion implanting an N type dopant for N-channel devices and ion implanting a P type dopant for P-channel devices.

17. The method of claim 14, wherein said sidewall spacers are formed by depositing a conformal chemical-vapor deposited insulating layer and anisotropically etching back to said semiconductor substrate, and resulting in an aspect ratio of said gaps between said gate electrodes of at least 6.0.

18. The method of claim 14, wherein said source/drain contact areas are formed by ion implanting an N^+ type dopant for N-channel devices and ion implanting a P^+ type dopant for P-channel devices.

19. The method of claim 14, wherein said self-aligned metal silicide layer is formed on said polysilicon gate electrodes and on said source/drain contact areas using a salicide process that uses a metal selected from the group that includes cobalt, nickel, and titanium.

20. The method of claim 14, wherein said metal silicide layer is formed to a thickness of between about 250 and 400 Angstroms.

21. The method of claim 14, wherein said sidewall spacers are silicon nitride and are partially removed using a hot phosphoric acid solution (H_3PO_4).

22. The method of claim 14, wherein said sidewall spacers are silicon oxide, and are partially removed using in-situ plasma etching in a high-density plasma etcher.

23. The method of claim 14, wherein said sidewall spacers are partially removed to provide an aspect ratio of said gaps of between 1.4 and 6.0.

24. The method of claim 14, wherein said interlevel dielectric layer is a phosphorus-doped silicon oxide deposited by chemical-vapor deposition to a thickness of at least about 9500 Angstroms.

25. The method of claim 24, wherein said interlevel dielectric layer includes a silicon nitride barrier layer having a thickness of about 600 Angstroms.

26. The method of claim 14, wherein said interlevel dielectric layer is a dielectric material having a low-dielectric constant.